MICROPROCESSOR AND INTERFACING

ES-301A

Time : Three Hours] [Maximum Marks : 75

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Describe the internal architecture of 8086 microprocessor with neat block diagram. **10**

   (b) Express how the physical address generated in 8086. **5**

2. (a) Examine all the signals available in the 8086 processor. **8**

   (b) How is the clock signal generated for 8086 ? Explain in detail. **7**

Unit II

3. (a) Describe the maximum mode configuration of 8086 with a neat diagram. Mention the functions of various signals. **7**

(b) For the given clock, draw the timing diagram for Read and write cycle in minimum mode operation and explain. **8**

4. (a) Interface the 8086 microprocessor with two 8K × 8 EPROM chips and two 8K × 8 RAM chips. Draw the necessary block diagram showing the interfacing of the memory with 8086. **10**

(b) Give the cell structures of PROM and E^2PROM memories. **5**

Unit III

5. (a) Define addressing mode. Describe in detail about each addressing mode with an example. **7**

(b) Mention an example for the 8086 instructions : **8**
AAA, CWD, JNBE, LAHF, MOVS, RCL, ROL, SAHF

6. (a) Generate the HEX codes for the following instructions : **8**

(i) Mov AX, BX

(ii) Mov AX, [BX] [SI].

(b) Write an assembly language program to search data in an array using 8086 instruction set. **7**

Unit IV

7. (a) Draw the complete interfacing diagram for interfacing an 8-bit channel A/D Converter like ADC 0808/0809 to an 8086 CPU. Test a sample, one at a time from each channel of analog inputs and display it at a special display port & wait for 2 seconds for each channel. 8

(b) Describe the 8255 programmable peripheral interface and its operating modes. What is the purpose of control word used in 8255 ? 7

8. (a) Interface a typical 12-bit DAC with 8255 and write a program to generate a triangular waveform of period 12 ms. The CPU runs at 4 MHz clock frequency. 8

(b) Describe the internal architectural diagram of the 8237 and explain how it functions as a DMA controller. 7